

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A clock generation circuit comprising:  
a plurality of former stage PLL circuits each configured to receive a reference signal  
and to generate an output synchronized to the received reference signal;  
a plurality of phase control circuits each configured to match a phase of an output  
from a former stage PLL circuit in the plurality of former stage PLL circuits to a phase of an  
output from another former stage PLL, and generate a phase matched output;  
a phase detector ~~for comparing~~ configured to compare said phase matched outputs to  
generate a control signal to said phase control circuits;  
a selection circuit configured to select one of the phase matched outputs from the  
plurality of former stage PLL circuits; and  
a latter stage PLL circuit linked in sequence to the plurality of former stage PLL  
circuits, and configured to receive the selected output and generate a clock that is  
synchronized with the selected phase matched output.

Claim 2 (Currently Amended): A clock generation circuit which selects one of a  
plurality of reference signals and generates a clock that is synchronized with a selected  
reference signal, the clock generation circuit comprising:

a plurality of former stage PLL circuits respectively provided for each of the plurality  
of reference signals, generating outputs that are respectively synchronized with a  
corresponding reference signal;  
a plurality of phase control circuits, respectively provided for each of the outputs from  
the plurality of former stage PLL circuits, for matching phase of an output from another one

of the plurality of former stage PLL circuits with phase of an output from one of the plurality of former stage PLL circuits to generate phase matched outputs;

a phase detector ~~for comparing~~ configured to compare said phase matched outputs to generate a control signal to said phase control circuits;

a selection circuit selecting one of the phase matched outputs; and

a latter stage PLL circuit linked in sequence to the plurality of former stage PLL circuits, for receiving the selected phase matched output and generating the clock.

Claim 3 (Previously Presented): The clock generation circuit according to claim 1, wherein the phase control circuits each include a ring counter and a selection circuit configured to select a multiphase output from the ring counter.

Claim 4 (Previously Presented): The clock generation circuit according to claim 1, wherein each former stage PLL circuit performs synchronization in frequency with the received reference signal, and

wherein the latter stage PLL circuit performs synchronization in phase with the selected reference signal,

the clock generation circuit further comprising, a divider circuit configured to divide the generated clock and to output a divided signal,

wherein the phase control circuit is further configured to match a phase of the divided signal to a phase of the selected reference signal

Claim 5 (Previously Presented): The clock generation circuit according to claim 4, wherein the phase control circuit is controlled based on a cycle of the selected reference signal.

Claim 6 (Previously Presented): The clock generation circuit according to claim 4, wherein the phase control circuit is controlled based on a divided cycle of the generated clock.

Claim 7 (Previously Presented): The clock generation circuit according to claim 2, wherein the phase control circuits each include a ring counter and a selection circuit configured to select a multiphase output from the ring counter.

Claim 8 (Previously Presented): The clock generation circuit according to claim 2, wherein each former stage PLL circuit performs synchronization in frequency with the corresponding reference signal, and

wherein the latter stage PLL circuit performs synchronization in phase with the selected reference signal,

the clock generation circuit further comprising, a divider circuit configured to divide the generated clock and to output a divided signal,

wherein the phase control circuit is further configured to match a phase of the divided signal to a phase of the selected reference signal.

Claim 9 (Previously Presented): The clock generation circuit according to claim 8, wherein the phase control circuit is controlled based on a cycle of the selected reference signal.

Claim 10 (Previously Presented): The clock generation circuit according to claim 8,  
wherein the phase control circuit is controlled based on a divided cycle of the generated  
clock.